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09/693,976	10/23/2000	Albert E. Casavant	A7675	8676

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EXAMINER	
PEREZ DAPLE, AARON C	

ART UNIT	PAPER NUMBER
2121	4

DATE MAILED: 02/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/693,976	Applicant(s) CASAVANT ET AL.	
	Examiner Aaron C Perez-Daple	Art Unit 2121	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Action is in response to Application filed 10/23/00, which has been fully considered.

2. Claims 1-18 have been presented for examination.

3. This Action is non-Final.

Information Disclosure Statement

4. Applicant is requested to provide an Information Disclosure Statement disclosing those references cited in the body of the specification (pgs. 1-5) and any additional references pertinent to the present application, as defined in 37 C.F.R. 1.56.

Drawings

5. Figures 1 and 17 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. Reference should be made to *circuit* simulation and design. The Examiner suggests, "Property-specific testbench generation framework for circuit design validation by guided simulation."

Claim Objections

7. **Claim 2** is objected to because of the following informalities: line 2 recites "said generation of said testbench" where it should recite --said generating a testbench automatically--. Line 17 ends in a semi-colon where it should end in a colon. Appropriate correction is required.

8. **Claim 4** is objected to because of the following informalities: line 4 recites "and" where it should recite --or--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. **Claims 1-13** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, lines 8-10 of claim 1 recite limitations in which actions are initiated based on whether the witness graph is "empty" or "not empty." The specification, while enabling for a method of pruning a witness graph, does not disclose nor discuss a witness graph having "empty" and "not empty" states. In contrast, the specification discloses an iterative method for "pruning" or selecting certain paths in a witness graph to arrive at a final witness graph [see top of page 28]. For the purpose of applying prior art, the Examiner interprets the limitations of lines 8-

11 to mean performing simulation with an automatically generated testbench until a conclusive result of property violation or property satisfaction is reached.

11. As dependent claims, claims 2-13 suffer from the same deficiencies as claim 1.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. **Claims 1-13** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Lines 8-10 of claim 1 recite limitations in which actions are initiated based on whether the witness graph is "empty" or "not empty." Because the specification does not disclose nor discuss a witness graph having "empty" and "not empty" states [see rejection under 35 U.S.C. 112, first paragraph, above], it is not clear how to interpret these limitations.

Moreover, referring to lines 12-21 of claim 1, for the case where the witness graph demonstrates more than one property, it is not clear how the witness graph can include paths only demonstrating the property violation or property satisfaction. Inherently, the witness graph would contain other paths for demonstrating the other properties. In this case Applicant appears to be claiming either multiple witness graphs or merely a portion of the witness graph. Additionally, even for the case with only one property, Applicant has not recited any steps directed at pruning the witness graph, which would be necessary for limiting the paths as claimed. Because "pruning" is not recited until claim 5, the Examiner interprets that claim 1 is intended to include the case without pruning. Based on this interpretation, the Examiner finds that any prior art teaching performing simulation with an

automatically generated testbench until a conclusive result of property violation or property satisfaction is reached, wherein the conclusive result is found by finding either counter-examples or paths demonstrating property satisfaction, meets all the limitations of lines 8-21 of claim 1.

14. As dependent claims, claims 2-13 suffer from the same deficiencies as claim 1.

15. **Claims 2 and 15** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, line 7 of claim 2 and line 5 of claim 15 recite "generating a vector generator module." Line 9 of claim 2 and line 8 of claim 15 recite "generating a monitor module." Based on the specification, it appears that the recited "modules" may comprise hardware or software. However, the modules already exist and therefore are not themselves generated in this step. Rather, the modules generate the vectors and monitor the results, as further recited in the claim. For the purpose of applying prior art, the Examiner interprets "generating" to mean --using--.

16. **Claim 14** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, lines 33-34 recite the limitation "until one of said paths in said witness graph has been completely simulated." It is not clear what comprises "completely simulated." The Examiner interprets that "until...completely simulated" means until producing a conclusive result from the set consisting of property violation and property satisfaction.

17. **Claim 18** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 18 recites the limitation "said pruning" in line 2. There is insufficient antecedent basis for this limitation in the claim. For the purpose of applying prior art, the Examiner interprets that claim 18 should depend from claim 17, not claim 16.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

19. **Claims 1, 15 and 16** are rejected under 35 U.S.C. 102(b) as being anticipated by Geist et al. ("Coverage-directed test generation using symbolic techniques," In Proceedings of the International Conference on Formal Methods in CAD, pgs. 143-158, Nov. 1996.) (hereinafter Geist).

As for claim 1, Geist discloses a method of verification for a design comprising:

providing a description of said design [section 1, first paragraph, "The goal of hardware...to expected results."];

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties [section 1, first paragraph, "The goal of hardware...to expected results."];

abstracting said design description to provide an abstract model of said design [section 3, second paragraph, "Building the FSM Model...are not relevant."];

generating a witness graph for said one or more correctness properties based on a deterministic analysis of said abstract model [section 3, second paragraph, "Building the FSM Model...are not relevant."] ;

determining a conclusive result from the set consisting of property violation and property satisfaction, when said witness graph is empty [section 3.2, paragraphs two and three, "Model checking [21] is a...covers the transition."]; and

generating a testbench automatically when said witness graph is not empty, and performing simulation with said testbench [section 3, paragraphs five to seven, "Generating Tests....the FSM model."];

wherein, when a property refers to universal path quantification, said witness graph includes paths demonstrating only said property violation, defining counter-examples [section 3.2, paragraphs two and three, "Model checking [21] is a...covers the transition."];

wherein, when said property refers to existential path quantification, said witness graph includes paths demonstrating only said property satisfaction, defining witnesses [section 3.2, paragraphs two and three, "Model checking [21] is a...covers the transition."];

wherein said conclusive result is said property satisfaction when said property refers to said universal path quantification [section 3.2, paragraphs two and three, "Model checking [21] is a...covers the transition."]; and

wherein said conclusive result is said property violation when said property refers to said existential path quantification [section 3.2, paragraphs two and three, "Model checking [21] is a...covers the transition."].

20. As for claim 15, Geist discloses an automatic test bench generation method for hardware design, said hardware design being described in a hardware description and including correctness criteria expressed as a correctness property [section 1, first paragraph, "The goal of hardware...to expected results."], said automatic test bench generation method comprising:

generating a witness graph based on said hardware description [section 3, second paragraph, "Building the FSM Model...are not relevant."];

determining, based on said witness graph, embedded constraints for guiding vector generation [section 3, fourth paragraph, "Semantic Control path...PCI transaction types."];

generating a vector generator module including said embedded constraints [section 3, paragraphs five to seven, "Generating Tests....the FSM model."]; and

generating, based on said correctness criteria, a monitor module for checking a correctness result with respect to said correctness property [section 3,2, paragraph 2, "Model checking...for test generation."].

21. As for claim 16, Geist discloses a method for assessing simulation coverage of a given set of simulation vectors for a given design, comprising:

providing a description of said design [section 1, first paragraph, "The goal of hardware...to expected results."];

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties [section 1, first paragraph, "The goal of hardware...to expected results."];

generating a witness graph for one or more of said correctness properties [section 3, second paragraph, "Building the FSM Model...are not relevant."]; and

determining coverage of said witness graph, using said given set of simulation vectors,

by marking entities visited by said given set of simulation vectors in said witness graph, said entities being selected from the set consisting of states, transitions and paths ["marking" is inherent for determining if a transition has occurred; section 3.1, "In practice, one...to cover both cubes."].

22. **Claim 16** is rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al. ("Toward formalizing a validation methodology using simulation coverage," Design Automation Conference, 1997. Proceedings of the 34th , June 9-13, 1997 Pages:740 - 745.) (hereinafter Gupta). As for claim 16, Gupta discloses a method for assessing simulation coverage of a given set of simulation vectors for a given design, comprising:

providing a description of said design [Fig. 1, design specification];

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties [Fig. 1, design specification];

generating a witness graph for one or more of said correctness properties [Fig. 2]; and

determining coverage of said witness graph, using said given set of simulation vectors,

by marking entities visited by said given set of simulation vectors in said witness graph, said entities being selected from the set consisting of states, transitions and paths [section 1, "An emerging paradigm...squashing and stalling)."].

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al. ("Toward formalizing a validation methodology using simulation coverage," Design Automation Conference, 1997. Proceedings of the 34th , June 9-13, 1997 Pages:740 - 745.) (hereinafter Gupta) in view of Geist.

As for claim 1, Gupta discloses a method of verification for a design comprising:

providing a description of said design [Fig. 1, design specification];

specifying correctness criteria for said design, wherein said correctness criteria are expressed as one or more correctness properties [Fig. 1, design specification];

abstracting said design description to provide an abstract model of said design [section 4.1, "We consider the implementation...in the implementation."];

generating a witness graph for said one or more correctness properties based on a deterministic analysis of said abstract model [Fig. 2].

Gupta further teaches generating a test bench automatically and determining a conclusive result from the set consisting of property violation and property satisfaction [section 2, "A test model can...a comparison of outputs."].

Under the interpretation presented under the 35 U.S.C. 112 rejections above, although obvious to one of ordinary skill in the art and arguably inherent in Gupta, Gupta does not explicitly disclose reaching a conclusive result by finding either counter-examples or paths demonstrating property satisfaction. Geist teaches reaching a conclusive result by finding either counter-examples or paths demonstrating property satisfaction [section 3.2, paragraphs two and three, "Model checking [21] is a...covers the transition."].

It would have been obvious to one of ordinary skill in the art to modify Gupta based on the teachings of Geist by reaching a conclusive result by finding either counter-examples or paths demonstrating property satisfaction, because this would provide coverage of the abstract model while ensuring that each test obeys the constraints [section 3.2, first paragraph, "Given a temporal...obeys that assertion."].

25. **Claims 2 and 3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Geist in view of Hollander (US 6,182,258 B1) (hereinafter Hollander).

As for claim 2, Geist discloses the method for verification as set forth in claim 1, wherein said generation of said tesbench comprises:

determining embedded constraints for guiding vector generation based on said witness graph [section 3, fourth paragraph, "Semantic Control path...PCI transaction types."];

determining priorities for guiding said vector generation based on said witness graph [section 3, third paragraph, "Defining a Coverage Model...our verification methodology."];

generating a vector generator module including said embedded constraints and said priorites [section 3, paragraphs five to seven, "Generating Tests....the FSM model."]; and

generating a monitor module, said monitor module checking said conclusive result [];

wherein, when said property refers to said universal path quantification, said vector generator module is generated so that said generated vectors are directed toward finding said counter-examples, and

wherein, when said property refers to said existential path quantification, said vector generator module is generated so that said generated vectors are directed toward finding said witnesses [section 3,2, paragraph 2, "Model checking...for test generation."]; and

said simulation of said design, using said generated test bench, comprises checking said monitor module for property violation or satisifation [section 3,2, paragraph 2, "Model checking...for test generation."].

Geist does not specifically disclose generating the vectors using random patterns and applying said constraints as a filter to select desireable ones of said random patterns. Hollander teaches generating vectors using random patterns and applying constraints as a filter to select desireable ones of said random patterns [col. 2, lines 58-61, "Parameter-driven test...meeting known parameters."].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Geist based on Hollander by generating the vectors using random patterns and applying said constraints as a filter to select desireable ones of said random patterns, because this would provide a method for generating suitable test vectors, as taught by Hollander [col. 2, lines 58-61, "Parameter-driven test...meeting known parameters."].

26. As for claim 3, Geist teaches a method of verication similar to that of claim 2, wherein:

said embedded constraints are derived from transition conditions in said witness graph [section 3, fourth paragraph, "Semantic Control path...PCI transaction types."]; and

said priorities are associated with transitions in said witness graph [section 3, third paragraph, "Defining a Coverage Model...our verification methodology."].

27. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Geist in view of Hollander and in further view of applicant's admitted prior art [pg. 24, lines 19-21].

Neither Geist nor Hollander specifically disclose generating priorities based on the methods recited in lines 3-5 of claim 4. However, applicant admits that these methods are known, as taught by the cited references <15, 17, 24 and 29>. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Geist and Hollander by generating priorities based on one or more of distance to targets, transition probabilities and simulator trace data, because these are known methods for prioritizing state space searching, as taught by Applicant.

Allowable Subject Matter

28. **Claim 17** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 6,477,683 B1, note Fig. 6; US 6,233,540 B1, note Fig. 3; US 6,243,852 B1, note col. 2; US 6,185,726 B1, note Fig. 5; US 6,321,363 B1, note iterative simulation method

using prior results; US 5,953,519, note automatic test bench generation; Fallah et al., "Simulation Vector Generation from HDL Descriptions for Observability-Enhanced Statement Coverage," Proc. 36th Design Automation Conf., 1999, pgs. 158-167, note discussion of coverage metrics with automatic test bench generation; Ganai et al, "Enhancing Simulation with BDDs and ATPG," Proc. Design Automation Conference, 1999, pgs. 385-390, note automatic test bench generation.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron Perez-Daple whose telephone number is 703-305-4897. The examiner can normally be reached on 9am - 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anil Khatri can be reached on 703-305-0282. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

2/2/04

Aaron Perez-Daple

ANIL KHATRI
SUPERVISORY PATENT EXAMINER